

16/12/16



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No. of Printed Pages: 2

**DOON UNIVERSITY, DEHRADUN**  
**End Semester Examination, December-2016**

**SEMESTER-I**

**MCA(Integrated): TMC-103[Digital Circuits & Systems]**  
**MSc CS(Integrated): CSC-102[Digital Electronics & System Design]**

*Time Allowed: 3Hours*

*Maximum Marks: 50*

*Note: Question paper is divided into three sections A, B & C. Marks distribution is given alongside. Follow the instruction as given in each section.*

**SECTION: A**

**Que-1**

**[Marks: 4\*1=04]**

- a) Draw the excitation table of J-K Flip-flop.
- b) Represent  $(25)_{10}$  in Excess-3 Code.
- c) Represent the following signed number in 2's complement method:
  - i) +25
  - ii) -25
- d) There are 15 address lines in a RAM. How many addressable locations are to load data into it. If this memory can accommodate 4 byte Word in any addressable location, calculate the storage capacity of this RAM.

**Que-2**

**[Marks: 3\*2=06]**

- a) Write Verilog and VHL Code for Full Adder.
- b) Convert  $(650.17)_8$  into decimal, binary, base 4 and hexadecimal.
- c) What do you understand by Combinational Circuits and Sequential Circuits? Discuss in detail.

**SECTION: B**

**[Marks: 5\*4=20]**

**Que-3** Design 16:1 MUX using 4:1 MUX.

**Que-4** Explain the operation of a 4 bit shift register.

Que-5 Convert the following :-

- a) JK to D      b) JK to T

Que-6

a) Simplify the Boolean expression using Boolean algebra rules.

$$Y = A'BC + AB'C + ABC' + ABC$$

b) Express it in standard POS Form

$$Y = (A+B)(A+C)(B+C')$$

Que-7

a) Design a full Adder using a decoder and additional gates.

b) Discuss some Applications of flip flops and registers.

### SECTION: C

Que-8

[Marks :2\*5=10]

- a) What do you understand by Counters. Design the circuit diagram of 4-bit Ring-Counter
- b) Design a 4-bit binary comparator that accept inputs A and B and gives three outputs. G,E and L.
- (i) Output G, when  $A < B$
  - (ii) Output E, when  $A = B$
  - (iii) Output L, when  $A > B$

Que-9

[Marks :1\*10=10]

Simplify using K-map, obtain minimal SOP equation and realize only by using NAND gates.

$$f(A, B, C, D) = \sum (1,2,3,8,9,10,11,14) + d(7,15)$$

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