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DOON UNIVERSITY, DEHRADUN

School of Technology

End Semester Examination: May-June, 2016

Program : MCA (Integrated) Semester: II

Course: STM-512 [Computer Architecture and Organization]

No. of Printed Pages: 3

Roll No._____

Time Allowed: 3 Hours ***Total Marks: 50***

Note: Question paper is divided into three sections A, B & C. Marks distribution is given alongside. Follow the instruction as given in each section.

SECTION: A

(10*1=10)

Attempt any ten of the following. Write your answer in about 50 Words.

Que-1

(i) Which bus is a bidirectional bus?

a) Address bus **b)** Data bus **c)** Address bus and data bus **d)** None of the above

(ii) In which of the following accessing method of I/O devices, the computer has an independent set of data, control and address buses, one for accessing memory and another for accessing I/O.

a) Isolated I/O method **b)** Memory mapped method **c)** Input-Output Processor **d)** DMA

(iii) Actual execution of instructions in a computer takes place in

a) ALU **b)** Control Unit **c)** Storage unit **d)** None of the above

(iv) The strobe method of asynchronous data transfer is not useful because

a) When source unit actives the strobe, there is no way of knowing whether the destination unit has received data

b) When destination unit actives the strobe, there is n way of knowing whether the Source unit has received data

c) Strobe control is not properly used by the other side of communicating device.

d) Processor is not able to respond the strobe control efficiently.

(v) The interrupt-initiated I/O method is used for

a) Transferring data to and from peripherals. **b)** Transferring data to and from memory.

c) Transferring data to processor only. **d)** All

(vi) What is a Computer Instruction?

(vii) What is locality of reference?

(viii) List important characteristics of RISC

(ix) Define Hit and Miss rate?

(x) What will be the width of address and data buses for a 512K * 8 memory chip?

(xi) Explain Start bit and stop bit in Asynchronous serial data transfer.

(xii) Why there are different addressing modes to access the instruction.

(xiii) How overflow is detected in Fixed Point Arithmetic.

SECTION: B

Attempt all of the following. Write your answer in about 250 Words.

(5*4=20)

Que-2 (a) Design the pin diagram of a typical RAM of 1GBX16 capacity

(b) What are some registers in a typical computer? Explain their purposes in detail.

OR

Starting from initial value of R=11011101, determine the sequence of binary values in R after a logical shift-left, followed by circular shift-right, followed by a logical shift right and a circular shift-left.

Que-3 (a) List and explain the steps involved in the execution of a complete instruction.

(b) Differentiate between direct and an indirect address instruction. How many references to memory are needed for each type of instruction to bring an operand into a processor register?

OR

Explain the IEEE Standard for floating point numbers in details.

Que-4 List all the Register Referencing Instruction for the Mano Machine along with their RTL statement.

OR

What is mapping in cache. What are different mapping techniques in Cache. discuss about any one.

Que-5 Register A holds the 4-bit binary 1010. Determine the value of A after logic operand B=1100 is applied in the following Micro operations

a. Selective Set **b.** Selective Complement **c.** Selective Clear

OR

Explain Booth's algorithm for multiplying binary integer in signed 2's complement representation

Que-6 Differentiate between

a) Cycle Stealing and Burst Transfer

b) Write Back and Write Through Policy

OR

Discuss the need of interface for I/O Devices

SECTION: C

Attempt all of the following. Write your answer in about 750 Words.

(4*5=20)

Que-7 Explain the function of DMA and the block diagram of DMS Controller in detail.

OR

Design and discuss the circuit for the RAM and ROM connection to the CPU.

Que-8 With example explain different types of instruction formats.

OR

Given the expression X=A*B + C*D . Explain how it will be executed in one address, two address and three address processors in an accumulator organization.

Que-9 An instruction is stored at location 300 with its address field at location 301. The address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is

(i) Direct **(ii)** Immediate **(iii)** Relative **(iv)**Register indirect **(v)** Index with R1 as the index register.

Que-10 What do you understand by RAID. What are the benefits of using RAID.

OR

Design the block diagram for the Hard-wired control unit of Mano Computer and discuss its working.
